CBCS SCHEME

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18EC56

Fifth Semester B.E. Degree Examination, Jan./Feb. 2023
Verilog HDL

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-1

1 a. Explain typical design flow for designing VLSI circuit using the flow chart. **(08 Marks)**

b. i) A 4-bit ripple carry adder (Ripple – Add) contains four 1-bit full adders (FA). Define the module FA. Do not define the internals or the terminal list. Define the module Ripple – Add. Do not define the internals or the terminal list. Instantiate four full adder of the type FA in the module Ripple-Add and call them fa0, fa1, fa2, and fa3.

ii) Define the module IS, using the module/endmodule keywords. Instantiate the modules MEM, Se, Xbar and call the instances mem1, se1 and Xbar 1, respectively. You do not need to define the internals. Assume that the module IS has no terminals. **(06 Marks)**

c. What are the two styles of stimulus applications? Explain each method in brief. **(06 Marks)**

OR

2 a. Explain the trends in HDL. **(04 Marks)**

b. With a hierarchical diagram of a 4-bit ripple carry counter, explain the design hierarchy **(10 Marks)**

c. What is the difference between a module and a module instance? Explain with an example. **(06 Marks)**

Module-2

3 a. Describe different methods of connecting parts to internal signals. **(06 Marks)**

b. Explain $ display, $ monitor, $ finish and $ stop system tasks with examples. **(08 Marks)**

c. What are the basic components of a module? Explain all the components of a verilog module with a neat diagram. **(06 Marks)**

OR

4 a. Declare the following variables in verilog.

i) An 8-bit vector net called a – in

ii) A 16-bit hexadecimal unknown number with all x's

iii) A memory MEM containing 256 words of 64 bits each

iv) A parameter cache-size equal to 512. **(04 Marks)**

b. With example explain different types of lexical conventions. **(08 Marks)**

c. Write verilog description of SR latch. Also write stimulus code. **(08 Marks)**

Module-3

5 a. Write a verilog dataflow description for 4-bit full adder with carry lookahead. **(06 Marks)**

b. What would be the output of the following

a = 4'b1010 , b = 4'b1111

i) a&b (ii) a&&b (iii) &a (iv) a>>1 (v) a>>>1

(vi) $y = \{2\{a\}\}$ (vii) $a \wedge b$ (viii) $z = \{a, b\}$ **(08 Marks)**

c. What re rise, fall and Turn-off delays? How they are specified in verilog? **(06 Marks)**

OR

6 a. A full subtractor has three 1-bit inputs x, y and z (previous borrow) and two 1-bit outputs D (Difference) and B (Borrow) the logic equations are

$D = \overline{X}\,\overline{Y}Z + \overline{X}Y\overline{Z} + X\overline{Y}\,\overline{Z} + XYZ$

$B = \overline{X}Y + \overline{X}Z + YZ$ **(06 Marks)**

Write veriolog description using dataflow modeling. Instantiate the subtractor inside a stimulus block and test all possible combinations of inputs X, Y and Z.

b. Discuss the And/or and Not gates with respect to logic symbols, gate instantiation and truth table. **(06 Marks)**

c. Design AND-OR-INVERT (AOI) based 4:1 multiplexer write verilog description for the same and its stimulus. **(08 Marks)**

Module-4

7 a. Explain the following assignment statements and non-blocking assignment statements with relevant examples. **(06 Marks)**

b. Write a veriolog program for 8-to-1 multiplexer using case statement. **(08 Marks)**

c. Give the differences between tasks and functions. **(06 Marks)**

OR

8 a. Explain sequential and parallel blocks with examples. **(06 Marks)**

b. Design a negative edge-triggered D-flipflp (DUFF) with synchronous clear, active high (D-FF clears only at a negative edge of clock when clear is high). Design a clock with a period of 10 units and test the D-flipflop. **(08 Marks)**

c. Write verilog program to call a function called calc-parity which computes the parity of a 32-bit data, [31-0] Data and display odd or even parity message. **(06 Marks)**

Module-5

9 a. Write a note on :

i) Force and release
ii) Defparam statement
iii) time scale
iv) file output. **(08 Marks)**

b. Write a note on verification of gate level netlist. **(04 Marks)**

c. With a neat flow chart explain computer Aided logic synthesis process. **(08 Marks)**

OR

10 a. What is logic synthesis? **(04 Marks)**

b. Interpret the following verilog constructs after logic synthesis.

i) The assign statement
ii) The if-else statement
iii) The case statement
iv) The always statement **(10 Marks)**

c. Write RTL description for magnitude comparator. **(06 Marks)**

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